IC Plus Corp.

ETHERNET PRODUCTS

IP1725 24+1-port Management Switch Controller with 24 PHYs inside (SOC_90nm, Green & Management)

General Description :

The IP1725 is a cost effective and fully integrated single chip. It integrates a 25-port switch controller, an 3X octal PHY transceiver and SSRAM. Each of PHY transceiver complies with 802.3u specification and HP-license Auto MDI/MDIX.

It supports full smart switch functions, including IGMP snooping, 4 priority queues, TOS, TCP/UDP port number priority, 802.1Q VLAN, port security, protocol filter/forwarding and bandwidth control.

Feature :

- S25 Ports 10/100Mb Ethernet Layer 2 Smart Switch
  - Built-in 24 PHYs
  - One MII interface
- Store & Forward, Share Memory Non_blocking Architecture
  - Built-in 2.5Mb SRAM (1.75Mb for packet buffer)
  - Max. length 1664B
- Wire-speed Operation On Every Port
- Head Of Line Blocking Prevention
- Flow Control Support
  - 802.3x compliant flow control in full duplex
  - Collision/Carrier_snese based backpressure in half duplex
- Internal 8K MAC Address Entities
  - CRC/direct hashing algorithm
  - Aging timer programmable (55s~251.6hr) < 4 %
  - Wire speed address learning and resolution
  - CPU accessible for security and static MAC
  - Learning enable/disable
- Sniffer Function Support (in/out/in+out)

- IGMP Snooping Support
  - Version 1 , 2
  - Snooping by Switch ASIC or external CPU
- Two Trunk Group Support
  - Two trunk groups, each trunk has 4 ports (max)
  - The ports belong to trunk group are configurable
  - Load balance based on (Port ID, DA , SA, DA/SA)
  - Link fault recovery
- VLAN (32 VLAN groups)
  - Port based
  - Tagged based
  - Tag remove/add/modify support
  - Special TAG support
  - Protected VLAN
  - Q-in-Q (double tag) support
- Class Of Service (CoS) Support
  - Port based
  - 802.1Q priority based tagged based
  - IP TOS based (IPv4/IPv6)
  - TCP/UDP port number based
  - Destination MAC address based
  - IP address based
  - 4 levels per port
  - WRR/FIFS/SP/SP+WRR
  - ACL based
- Broadcast Storm Control
  - Broadcast rate control per port selectable
  - With option to drop all ARP to CPU
  - Also has ARP and ICMP storm control
- Multi-cast/unknown DA frames can be counted
- Port Security
  - MAC based
  - IP(DIP/SIP) based (IPv4 32 bit only
  - TCP/UDP port based
  - Port based
- Bandwidth Control
  - 32K bpsxN 256 levels
  - 512K bpsxN 256 levels
  - With flow control/Without flow control
  - WAN port control support
- Support SMI Interface Auto-polling
  - Speed, Duplex, Flow control, Link
  - CPU accessible (interrupt support)

- CPU R/W PHY register
- Out Queue Aging Function
  - From 100 ms to 6.3 sec selectable
- Spanning Tree Protocol Port State Support
  - Discard/Block/Learning/Forwarding four states support
  - Forwarding STP frame to CPU port
  - RSTP support
- Support 16 ACL Entities Based On
  - Ingress port or VLAN
  - Destination/Source IP (specific or range)
  - TCP/UDP Destination/Source port number (specific, > 1023, <=1023)
  - Forwarding STP frame to CPU port
  - Action : forward, to CPU, drop, priority, Q-in-Q tag
- Configuration
  - Pin initial setting
  - 2-wire serial interface for configuration EEPROM
  - 2-wire serial interface for low cost smart system application
- Per Port 2 Counter (32 bit x 2) Selectable
  - RX/TX packet count
  - CRC error packet count
  - Drop packet count
  - Collision count
- LED
  - Direct mode
  - 2-wire serial mode
- Support Auto Test Function For Mass-production
  - Auto generate test frames
  - Shown the result on LED output
- Interrupt Pin For PHY Mode/Link/SMI R/W
  - Complete notification
- Build-in SRAM Self Test (BIST)
- Build-in Oscillator Circuit, Only One 25 MHz Crystal Needed
- IO Voltage Selectable (3 groups)
- 90 nm Process, 208 Pin EDHS-QFP